A Parallel Architecture for Motion Estimation in HEVC Encoder

Nowadays, the use of hardware/software codesign has grown dramatically in the design of embedded systems since it can improve the processing power, system efficiency, and the total cost of production. In this method, some parts of the system are implemented in hardware and the other parts implemented in software in order to satisfy the system constraints, including power consumption, area and processing time. In this project, we proposed a parallel architecture for motion estimation in HEVC encoder. In the proposed method, the motion estimation part of the encoder which has a high computational complexity, implemented in hardware and the computational complexity of this part is improved using parallel processing. The hardware implementation of motion estimation part is much less complex than the adopted HM reference software, making it more suitable for embedded systems.

The percentage of required time for the main units of HEVC codec relative to the total processing time in Software implementation

The processing unit	Execution Time (%)
Motion Estimation (Encoder Side)	8.09

The total required time for motion estimation in hardware implementation for one frame and various block sizes

Block size	Total required time in hardware
4 × 4	85 s
8 × 4	42 s
16 × 16	5.3 s
64 × 32	0.6 s
64 × 64	0.3 s